EAST - [~default1.wsp:1]

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DBs | USPAT; US-PGPUB; EPO; JPO

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1	BRS	L1	50	("5565371" "6172915" "5295107"	USPAT ; US-PG	2003/05/04
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of approximately 2 to 3 V is applied to the source so that essentially no current will flow from the source to the substrate. In addition, the control gate is also appropriately biased so that there will be essentially no flow of channel current either. When a reverse bias of approximately 14 V is then applied between the drain and substrate, a current-avalanche effect is produced in the vicinity of the drain junction beneath the gate oxide film. This avalanche comprises for example hot positive-carrier holes which in turn become injected into the floating gate, thereby neutralizing the previously channel-injected opposite-carrier charge.

More specifically, as shown in FIG. 6*a*, the switch I is first closed and the switch II is opened, so that $V_G=V_B=0$ V and $V_S=2$ V are applied to the cell. Next, as shown in FIG. 6*b*, the switch II is closed, and a pulse of $V_D=14$ V is applied to the drain 42, thereby effecting erasure. Thus by appropriate alterations in applied voltages, not only the writing of data but also the erasing of data can be accomplished electrically.

FIG. 7 shows the relationship between applied erase-pulse duration-time T_E and resultant V_T under these conditions. It is seen from FIG. 7 that in the case of a cell in which V_{TA} is 6.6 V, the value of V_T drops to 2.0 V after a 50-msec application, so that the cell almost returned to its original, pre-writing state. After approximately this 50 msec, moreover, the erasure curve becomes essentially asymptotic.

6, the drain voltage V_D breakdown occurs increa increased from 1 V to 3 biasing of the source with it possible to maintain th location which contribu the occurrence of breakd result in the flow of an e

It may be noted pare affirmative positive biasir the only way of avoidi breakdown. This objecti biasing the substrate V_B even if the source potenti floating, the subject sour positive potential during between the source and accordingly be the same source biasing.

FIG. 9 next shows the characteristics with the s Here, the floating gate parameter, and the subst Figure shows that avala lower drain voltages as this is that the electric f drain junction increases i potential V_{FG} drops.